

PulseNet Pin Descriptions:

Power, ground, reference voltages (37):

AGND -- analog ground (8)
AVdd -- analog power (8); 2.5 V
GND -- ground (7)
Vdd -- power (7); 2.5 V
Vref[6:0] - reference voltages (7), perhaps 2.05 V, 1.98 V, 1.94 V, 1.86 V, 1.70 V, 1.38 V, 1.06 V

Note: analog and digital power/ground structures might be combined depending on the result of a power/ground-bounce simulation

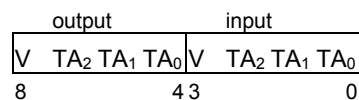
Analog inputs (32):

A0A..A15A, A0B..A15B (32) -- AC-coupled PMT anodes; note that An{A,B} are a pixel pair (where $0 \leq n \leq 15$)

SETI I/O (7):

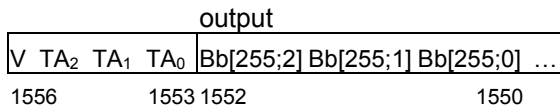
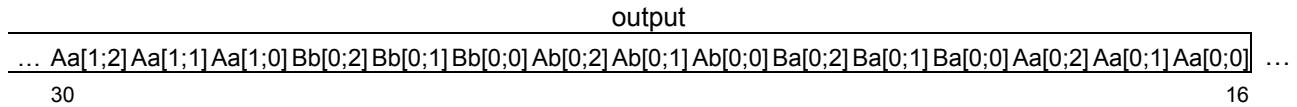
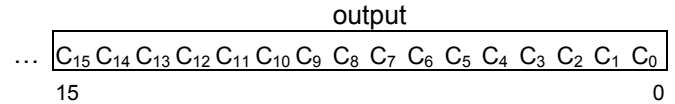
en (input) -- enable; when high, other SETI pins are active; when low, they are tri-stated (if outputs) or ignored (if inputs)
rst (input) -- reset; clears CoincL2 and CoincL3
SETIClk (input) -- clock for bringing programming data into the SETI module and coincident pulse data off chip; slow, microcontroller speed
ProgIn (input) -- used to clock in programming bits for SETI module
data (output) -- used to clock out coincident pulse data
CoincL2 (output) -- two-state flag that goes high when a coincidence is recorded; it goes low on the rising edge of rst
CoincL3 (output) -- same as CoincL2, except the two states are high and high-Z

Functional description: When en is high, the chip is in "SETI I/O mode" and it can be initialized by bringing rst high. After lowering rst, one programs the module by clocking data in on ProgIn on the rising edge of SETIClk. It expects the first three bits to be the threshold address in binary (veto = 0, 1st level = 1, etc., 2nd level = 2; 111 -> 000) with the LSB first. The next bit, when high, enables "veto mode" -- an initial coincidence is rejected if the veto level goes high within 32 cycles of the coincident event. Additional programming bits may follow (such as a bit to disable half of the samplers or a bit to bypass half of the memory), but that is still up in the air. When the programming is done, the next 4 clocks cause the previously entered data to be echoed back on the data pin (on the rising edge of SETIClk). This is included as a debug tool/sanity check. That bit sequence is illustrated below.



When en is lowered, the chip goes into "coincidence detection mode". (Note that the astronomy counters continue to function when PulseNet is in either mode. The chip modules are essentially independent.) When a coincidence is detected, CoincL2 and CoincL3 go high. The outside world should wait for the memory to fill up before trying to clock data out (this time is equal to the memory depth divided by twice the on-chip frequency). The data appear on the data pin when SETIClk is toggled. The first 16 bits say whether or not each of the 16 pixel pairs received a coincidence (high = coincidence received). This should only be one of sixteen but this scheme allows reporting on the addresses of multiple coincidences (priority for data storage in the memory bank is given to pixel pairs with lower address values). The next 6x256 bits are the Gray-encoded outputs of the samplers from the coincident pixel pair. Their order is shown below.

Note that $Nn[i;j]$ refers to the j th gray-encoded bit that is i th in the time sequence from the N -member of the pixel pair that was sampled on the n -edge of the clock.



When all of this data is clocked out, additional clocks echo the programming bits (as they were entered in programming mode). The user can clear the coincidence flags by toggling `rst` high. If no programming bits are clocked in, then the old settings will remain. The chip will go back into "coincidence detection mode" when `en` goes low (assuming that the flags were cleared).

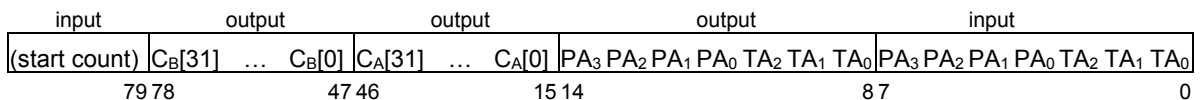
Astronomy I/O (5):

- AstEn (input) -- astronomy enable; when high, all other Ast pins are active; when low, they are tri-stated (if outputs) or ignored (if inputs)
- AstRst (input) -- reset; zeros the internal counters (astronomy counters and clock counter)
- AstIn (input)-- used to clock in programming bits for astronomy module
- AstOut (output) -- used to output counter values
- AstClk (input) -- externally driven clock (slow, microcontroller speed) used with AstOut and AstIn

Functional description: When AstEn is high, it can be initialized by bringing AstRst high. After lowering AstRst, the module listens on AstIn and AstClk. On the rising edges of AstClk, 7 programming bits are clocked in on AstIn. The first three bits are the astronomy threshold address in binary (as above) with the LSB first. The next four bits are the pixel pair address, again in binary with the LSB first. On the next 7 clock cycles, the module will echo the threshold address and the pixel pair address, in the order in which the bits were received (as a sanity check).

On the next 64 clock cycles, the astronomy module will output the values on the counters -- 32 bits each, in binary (LSB first, 111 = none), with the A-channel counter first. On the next rising edge of the clock (the 79th), the counters in the astronomy module start counting. They continue to count as AstEn is lowered, but stop on the next rising edge of AstEn.

The bit sequence for the programming and readout procedure is shown in the table below.



Miscellaneous (3):

- RingOsc (output) -- ring oscillator output used for diagnostics (~3 Mhz)
- clkn/clkp (2, input) -- differential clock inputs (~500 MHz)