

TABLE 8.9. D-TYPE REGISTERS AND LATCHES<sup>a</sup>

Type				Bits	Pins	Enable	Reset <sup>b</sup>	Broadside <sup>c</sup>	Q/Q <sup>d</sup>	Output <sup>e</sup>	Comments
true	inverted	D-type	latch								
'173	–	–	–	4	16	–	A	•	–	3S	
'175	'375	'175	'375	4	16	–	A	–	•	2S	
'298	–	–	–	4	16	–	–	•	–	2S	MUXed input
'379	–	'379	–	4	16	•	–	–	•	2S	sim to '175, but CLR→EN
'398	–	'398	–	4	20	–	–	–	•	2S	MUXed input
'399	–	–	–	4	16	–	–	–	–	2S	MUXed input
'174	–	–	–	6	16	–	A	–	–	2S	
'378	–	–	–	6	16	•	–	–	–	2S	sim to '174, but CLR→EN
'273	–	–	–	8	20	–	A	–	–	2S	
'374	'373	'534	'533	8	20	–	–	–	–	3S	
'377	–	–	–	8	20	•	–	–	–	2S	sim to '374, but 3S→EN
–	'412	–	'432	8	24	•	A	–	–	3S	Intel 8212; status bit
'574	'573	'564	'563	8	20	–	–	•	–	3S	broadside '374/3; also '576/'580
'575	–	'577	–	8	24	–	S	•	–	3S	'574 with synch CLR
'825	'845	'826	'846	8	24	•	A	•	–	3S	Am29825
'823	'843	'824	'844	9	24	•	A	•	–	3S	Am29823
'821	'841	'822	'842	10	24	–	–	•	–	3S	Am29821; 10-bit '374
'396	–	–	–	4+4	16	–	–	–	–	2S	cascaded 4-bit reg; 8-bit out
'874	'873	'876	'880	4+4	24	–	A	•	–	3S	
'878	–	'879	–	4+4	24	–	S	•	–	3S	'874 with synch CLR
–	'604	–	–	8+8	28	–	–	–	–	2S	MUXed input; '605 is OC
–	'606	–	–	8+8	28	–	–	–	–	2S	glitch-free '604; '607 is OC

(a) see also "TRANSCIEVERS," some of which have latches. (b) A – asynchronous; S – synchronous. (c) broadside (flow-through) pinout. (d) both true and complemented outputs. (e) 2S – push-pull (2-state) output; 3S – 3-state output.