

TABLE 8.5. TRANSCEIVERS

Type		Bits	Pins	Registers	Output drive <sup>a</sup>		Enables		Broadside <sup>c</sup>	Comments <sup>d</sup>
true	inv				sink (mA)	source (mA)	pol	mode <sup>b</sup>		
'243	'242	4	14	–	24	15	L,H	LR	•	
'245	–	8	20	–	24	15	L	DE	•	
'543	'544	8	24	2			L	LR	•	
'545	–	8	20	–			L	DE	•	
'550	'551	8	28	2			L	LR	–	Am2950/1
'552	–	8	28	2			L	LR	–	+ parity gen
'588	–	8	20	–			L	DE	•	IEEE-488 term resistors
'623	'620	8	20	–	24	15	L,H	LR	•	'621/2 are OC
'639	'638	8	20	–	24	15	L	DE	•	3-state in one dir, OC in other
'643	–	8	20	–	24	15	L	DE	•	Q and Q' outputs; '644 is OC
'645	'640	8	20	–	24	15	L	DE	•	'641/2 are OC
'646	'648	8	24	2	24	15	L	DE	•	'647/9 are OC
'652	'651	8	24	2	24	15	L,H	LR	•	'654/3 are 3S one dir, OC other
'657	–	8	24	–			L,H	DE	•	+ parity gen
'2623	'2620	8	20	–	12	2	L,H	LR	•	25Ω output resistors
'2645	'2640	8	20	–	12	2	L	DE	•	25Ω output resistors
2952	'2953	8	24	2	24	6.5	L	LR	•	'2950/1 have handshake

(a) for LS-family devices. (b) DE - DIRection and ENable inputs; LR - separate Left and Right enables.

(c) broadside (flow-through) pinout. (d) all are 3-state, unless stated otherwise.