

TABLE 8.11. SHIFT REGISTERS

Type	Bits	Pins	Serial/parallel		Direction	Latches ^a	Reset ^b	Output ^c	Comments ^d
			input	output					
'95	4	14	P/S	P	R	-	-	2S	
'194	4	16	P/S	P	R/L	-	A	2S	
'195	4	16	P/JK	P	R	-	A	2S	
'295	4	14	P/S	P	R	-	-	3S	
'395	4	16	P/S	P/S	R	-	A	3S	
'671	4	20	P/S	P	R/L	O	A	3S	output MUXed: SR or latch; reset SR only
'672	4	20	P/S	P	R/L	O	S	3S	'671 with synch CLR
'96	5	16	P/S	P	R	-	A	2S	high load only
'91	8	14	2S	2S	R	-	-	2S	
'164	8	14	2S	P	R	-	A	2S	
'165	8	16	P/S	2S	R	-	-	2S	
'198	8	24	P/S	P	R/L	-	A	2S	
'299	8	20	P/S	P/S	R/L	-	A	3S	common I/O pins
'322	8	20	P/S	P/S	R	-	A	3S	common parallel I/O
'323	8	20	P/S	P/S	R/L	-	S	3S	'299 with synch reset
'589	8	16	P/S	S	R	I	-	3S	power-up clear (SR only)
'594	8	16	S	P/S	R	O	2A	2S	'599 is O/C; separate resets
'595	8	16	S	P/S	R	O	A	3S	'596 is O/C; reset SR only
'597	8	16	P/S	S	R	I	A	2S	reset SR only
'598	8	20	P/2S	P/S	R	I	A	3S	common parallel I/O; reset SR only
'673	16	24	S	P/S	R	O	A	2S	common serial 3S I/O; reset latch only; CS, R/W
'674	16	24	P/S	S	R	-	-	3S	common serial 3S I/O; CS, R/W
'675	16	24	S	P/S	R	O	-	2S	CS, R/W
'676	16	24	P	S	R	-	-	2S	CS

(a) O - at output; I - at input. (b) A - asynchronous; S - synchronous. (c) 2S - 2-state (totem pole); 3S - 3-state.

(d) CS - chip select input; R/W - read/write input.