

TABLE 8.10. COUNTERS

Type		Bits	Pins	Clock ^a	Load ^a	Reset ^a	U/D ^b	Direct/ latch ^c	Output ^d	Comments
binary	BCD									
'93	'90	4	14	A	-	A	-	D	2S	non-st'd Vcc, gnd; '92 is modulo-12
'161	'160	4	16	S	S	A	-	D	2S	
'163	'162	4	16	S	S	S	-	D	2S	
'169	'168	4	16	S	S	-	•	D	2S	
'191	'190	4	16	S	A	-	•	D	2S	
'193	'192	4	16	S	A	-	•	D	2S	separate U/D clock inputs
'197	'196	4	14	A	A	A	-	D	2S	
'293	'290	4	14	A	-	A	-	D	2S	'93 with st'd Vcc, gnd
'561	'560	4	20	S	B	B	-	D	3S	
'569	'568	4	20	S	S	B	•	D	3S	25LS2569/8
'669	'668	4	16	S	S	-	•	D	2S	improved '169
'691	'690	4	20	S	S	A	-	B	3S	
'693	'692	4	20	S	S	S	-	B	3S	
'697	'696	4	20	S	S	A	•	B	3S	
'699	'698	4	20	S	S	S	•	B	3S	
'4516	'4510	4	16	S	A	A	•	D	2S	
-	'4017	5	16	S	-	A	-	D	2S	decoded 1-of-10 outputs
'4024	-	7	14	A	-	A	-	D	2S	
'69	'68	8	16	A	-	A	-	D	2S	
'269	-	8	24	S	S	-	•	D	2S	skinny-DIP
'393	'390	8	14/16	A	-	A	-	D	2S	dual '93/'90
'461	-	8	24	S	S	S	-	D	3S	PAL
'469	-	8	24	S	S	-	•	D	3S	PAL
'579	-	8	20	S	S	B	•	D	3S	8 bidirectional in/out lines
'590	-	8	16	S	-	A	-	L	3S	
'591	-	8	16	S	-	A	-	L	OC	
'592	-	8	16	S	A	A	-	L	2S	8 inputs, 1 output (MAX CNT)
'593	-	8	16	S	A	A	-	L	3S	8 bidirectional in/out lines
'779	-	8	16	S	S	-	•	D	3S	8 bidirectional in/out lines
'867	-	8	24	S	S	A	•	D	2S	skinny-DIP
'869	-	8	24	S	S	S	•	D	2S	skinny-DIP
'4520	'4518	8	16	S	-	A	-	D	2S	pos or neg edge clk
'40103	'40102	8	16	S	B	A	D	D	2S	
'4040	-	12	16	A	-	A	-	D	2S	
'4020	-	14	16	A	-	A	-	D	2S	
'4060	-	14	16	A	-	A	-	D	2S	

(a) A - asynchronous; all A clock inputs count on neg edge. S - synchronous; all S clock inputs count on positive edge. B - both. (b) D - count down only. (c) B - both. (d) 2S - 2-state (totem-pole); 3S - 3-state.